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<TR><TD>(54)<B> IMAGE SIGNAL PROCESSOR AND IMAGE SIGNAL PROCESSING
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METHOD
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(57)Abstract:
PROBLEM TO BE SOLVED: To provide an image signal processor which can reduce failure of motion detection that occurs upon IP conversion of high speed scrolling screen, and its method.
SOLUTION: The processor has a DSP 11. It executes motion detection, which is executed when creating interpolation data for lines without data upon IP conversion, according to the motion detection result of the data created by interpolating between the data of the current field and the data delayed by 2 fields, and between the data of the current field and the data delayed by 1 field, and the motion detection result of the previous field. It creates interpolation data by means of intra-field interpolation from the data delayed by 1 field, for the moving space. As for the static space, it creates interpolation data by means of inter-field interpolation from the current field. When the resulting value of intra-field interpolation and that of inter-field interpolation exceed the certain threshold, then it regards it to be the moving space, and executes intra-field interpolation. When the result of motion detection for the previous field is static, it makes the threshold value larger, and when it is moving, it makes it smaller.

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<HR>CLAIMS
<HR>[Claim(s)]

[Claim 1]

Motion detection is performed about Rhine where the data of an interlace signal do not exist.
Interpolation data are created about Rhine where the data of an interlace signal do not exist.
It is the picture signal processor which changes image data into a progressive signal from an interlace signal based on the interpolation data concerned.
The motion detection at the time of changing image data into a progressive signal from an interlace signal
Based on the data and the motion detection result of the front field which were interpolated and created from the present field, the data of 2 field delay, and the data of 1 field delay, it carries out for every pixel.
Interpolate the field currently moved in the field from the data of 1 field delay, it creates interpolation data, and a stationary field The data of the present field Or the picture signal processor which has a processing means to create interpolation data from the data of 2 field delay or the data of the present field, and the data of 2 field delay.

[Claim 2]

The above-mentioned processing means is a picture signal processor according to claim 1 which regards it as a motion field and performs interpolation in the field when the result of the interpolation in the field and the result of interpolation between the fields exceed a predetermined threshold.

[Claim 3]

The above-mentioned processing means is a picture signal processor according to claim 2 which adjusts the above-mentioned threshold automatically according to the result of motion detection of the front field.

[Claim 4]

The above-mentioned processing means is a picture signal processor according to claim 3 which will make a threshold small if the motion detection result of the front field is quiescence, and the above-mentioned threshold will be enlarged and it will come to move.

[Claim 5]

The above-mentioned processing means is a picture signal processor according to claim 1 which has the SIMD control processor which made the element processor many juxtaposition in one dimension.

[Claim 6]

The above-mentioned processing means is a picture signal processor according to claim 2 which has the SIMD control processor which made the element processor many juxtaposition in one dimension.

[Claim 7]

The above-mentioned processing means is a picture signal processor according to claim 3 which has the SIMD control processor which made the element processor many juxtaposition in one dimension.

[Claim 8]

The above-mentioned processing means is a picture signal processor according to

claim 4 which has the SIMD control processor which made the element processor many juxtaposition in one dimension.

[Claim 9]

The SIMD control processor which many arranged the above-mentioned element processor in parallel in one dimension is a picture signal processor according to claim 5 which is bit processing.

[Claim 10]

The SIMD control processor which many arranged the above-mentioned element processor in parallel in one dimension is a picture signal processor according to claim 6 which is bit processing.

[Claim 11]

The SIMD control processor which many arranged the above-mentioned element processor in parallel in one dimension is a picture signal processor according to claim 7 which is bit processing.

[Claim 12]

The SIMD control processor which many arranged the above-mentioned element processor in parallel in one dimension is a picture signal processor according to claim 8 which is bit processing.

[Claim 13]

Motion detection is performed about Rhine where the data of an interlace signal do not exist.
Interpolation data are created about Rhine where the data of an interlace signal do not exist.
It is the picture signal art which changes image data into a progressive signal from an interlace signal based on the interpolation data concerned.
The motion detection at the time of changing image data into a progressive signal from an interlace signal
Carry out based on the data and the motion detection result of the front field which were interpolated and created from the present field, the data of 2 field delay, and the data of 1 field delay, and the field currently moved
Interpolate in the field from the data of 1 field delay, create interpolation data, and a stationary field The data of the present field
Or the picture signal art which interpolates between the fields from the data of 2 field delay or the data of the present field, and the data of 2 field delay, and creates interpolation data.

[Claim 14]

It is the picture signal art according to claim 13 which regards it as a motion field and performs interpolation in the field when the result of the interpolation in the field and the result of interpolation between the fields exceed a predetermined threshold.

[Claim 15]

The picture signal art according to claim 14 which adjusts the above-mentioned threshold according to the result of motion detection of the front field.

[Claim 16]

The picture signal art according to claim 15 which will make a threshold small if the motion detection result of the front field is quiescence, and the above-mentioned threshold will be enlarged and it will come to move.

<HR>DETAILED DESCRIPTION
<HR>[Detailed Description of the Invention]

[0001]

[Field of the Invention]

This invention relates to the picture signal processor which is applied to a picture signal processor, especially changes an interlace signal into a progressive signal (IP conversion), and its approach.

[0002]

[Description of the Prior Art]

Many public picture signals, such as television and video, are interlaces. On the other hand, a computer signal is progressive, for example, in order to display the image of a computer, and the image of television on the same computer display as coincidence, it must change an interlace signal into progressive. Moreover, if thin striping is in an image, a flicker will arise from the description, but by the progressive signal, since an interlace signal does not have such a thing and is displayed finely, recently, it has some which perform conversion to progressive from an interlace inside, and are displayed by progressive also with a television set for home use.

[0003]

About IP conversion, an INTARESU signal constitutes one frame from the two fields with the Rhine data in mutually shifted every other line, as shown in
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.
On the other hand, as a progressive signal is shown in
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, all the Rhine data exist from the beginning (choked up).
When changing into progressive from an interlace signal, since only the data in every other line exist, by interlace, interpolation data are made and outputted about Rhine without data.

[0004]

Generally, although this interpolation data has various ways of making, as shown in
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, it detects by usually moving, and divides into a motion area and a quiescence field, interpolation data are created from the data in the field about a motion area, and the method of bringing the data of the same Rhine of the front field as it is is used about a quiescence field.
And the motion detection processing at the time of performing IP conversion conventionally had compared and judged the data of the present field and 2 field delay.

[0005]

[Problem(s) to be Solved by the Invention]

However, as mentioned above, when an image an alphabetic character telop carries out [an image] high-speed scrolling was in the former image which performs IP conversion by the conventional approach, it had become the sensibility to which motion detection fails and scrolling of an alphabetic character telop dragged on.

[0006]

For example, when two rods scroll and go to a high speed, it comes to be shown in
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.

In addition,

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sets and it is illustrating sideways for convenience.

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(A) --

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(C) moves 2 field eye,

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(D) moves 3 field eye for 1 field eye, and

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(B) shows the result of IP conversion to the result of detection, and

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(E).

Here, E lines of 2 field eye are interpolated.

[0007]

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(D) which shows the result of motion detection -- setting -- * -- the difference of 1 field eye and 3 field eye -- an absolute value -- being shown -- + -- motion area space -- being large -- it is shown.

And in the result of IP conversion based on the conventional approach, about Rhine of O, 2 field eye remains as it is, about Rhine of E, it interpolates from 2 field eye and, as for the motion field (*, +), the quiescence field ( ) uses 3 field eye as it is.

however, it is shown in

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TARGET="tjitemdrw">drawing 10</A>

(E) in this case -- as -- the space of motion detection -- being large -- even if it extends, it cannot avoid completely but has become an error.

[0008]

Moreover, while the longitudinal direction is carrying out IP conversion to the result of IP conversion based on the conventional approach by LAP similarly, an error is conspicuous on a screen which an alphabetic character telop scrolls at a high speed.

[0009]

For example, when two rods scroll and go to a high speed, it comes to be shown in
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(C) moves 2 field eye,
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(D) moves 3 field eye for 1 field eye, and
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(B) shows the result of IP conversion to the result of detection, and
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(E).
<A
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TARGET="tjitemdrw">drawing 11</A>
(D) which shows the result of motion detection also in this case -- setting -- * -- the difference of 1 field eye and 3 field eye -- an absolute value -- being shown -- + -- motion area space -- being large -- it is shown.
And in the result of IP conversion based on the conventional approach, it interpolates from 2 field eye and, as for the motion field (*, +), the quiescence field ( ) uses 3 field eye as it is.
however, it is shown in
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TARGET="tjitemdrw">drawing 11</A>
(E) also in this case -- as -- the space of motion detection -- being large -- even if it extends, it cannot avoid completely but has become an error.

[0010]

This invention is made in view of this situation, and the purpose is in offering the picture signal processor which can mitigate the breakdown of the motion detection generated in case IP conversion of the screen of high-speed scrolling is carried out, and its approach.

[0011]

[Means for Solving the Problem]

In order to attain the above-mentioned purpose, this invention about Rhine where the data of an interlace signal do not exist
About Rhine where motion detection is performed and the data of an interlace signal do not exist
It is the picture signal processor which creates interpolation data and changes image data into a progressive signal from an interlace signal based on the interpolation data concerned.
The motion detection at the time of changing image data into a progressive signal from an interlace signal
Based on the data and the motion detection result of the front field which were interpolated and created from the present field, the data of 2 field delay, and the data of 1 field delay, it carries out for every pixel.
Interpolate the field currently moved in the field from the data of 1 field delay, it creates interpolation data, and a stationary field The data of the present field Or it has a processing means to create interpolation data from the data of 2 field delay or the data of the present field, and the data of 2 field delay.

[0012]

Moreover, in this invention, when the result of the interpolation in the field and the result of interpolation between the fields exceed a predetermined threshold, it considers that the above-mentioned processing means is a motion field, and it performs interpolation in the field.

[0013]

Moreover, in this invention, the above-mentioned processing means adjusts the above-mentioned threshold automatically according to the result of motion detection of the front field.

[0014]

Moreover, in this invention, the above-mentioned processing means will make a threshold small, if the motion detection result of the front field is quiescence, and the above-mentioned threshold will be enlarged and it will come to move.

[0015]

Moreover, in this invention, the above-mentioned processing means has the SIMD control processor which made the element processor many juxtaposition in one dimension.

[0016]

Moreover, in this invention, the SIMD control processor which many arranged the above-mentioned element processor in parallel in one dimension is bit processing.

[0017]

moreover, this invention about Rhine where the data of an interlace signal do not exist
About Rhine where motion detection is performed and the data of an interlace signal do not exist
It is the picture signal art which creates interpolation data and changes image data into a progressive signal from an interlace signal based on the interpolation data concerned.

The motion detection at the time of changing image data into a progressive signal from an interlace signal
Carry out based on the data and the motion detection result of the front field which were interpolated and created from the present field, the data of 2 field delay, and the data of 1 field delay, and the field currently moved
It interpolates in the field from the data of 1 field delay, and interpolation data are created, and a stationary field is interpolated between the fields from the data of the present field, the data of 2 field delay or the data of the present field, and the data of 2 field delay, and creates interpolation data.

[0018]

According to this invention, motion detection at the time of carrying out IP conversion is performed based on the data and the motion detection result of the front field which were interpolated and created from the present field, the data of 2 field delay, and the data of 1 field delay.
And the field currently moved is interpolated in the field from the data of 1 field delay, and interpolation data are created.
On the other hand, a stationary field is interpolated between the fields from the data of the present field, and interpolation data are created.
Moreover, when the result of the interpolation in the field and the result of interpolation between the fields exceed a predetermined threshold, it is regarded as a motion field and interpolation in the field is performed.
Moreover, it is adjusted, and if it moves and becomes, it will be adjusted so that a threshold may become small, so that a threshold may become large, if motion detection of the front field is quiescence.
Thereby, when quiescence continues, a threshold becomes higher and higher, it flickers and IP conversion can be performed that there is nothing.

[0019]

[Embodiment of the Invention]

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TARGET="tjitemdrw">Drawing 1</A>
is the block diagram showing 1 operation gestalt of the picture signal processor concerning this invention.

[0020]

This picture signal processor 10 has the memory 12 and 13 for generating the digital signal processor (DSP) 11 and 1 field delay as a processing means as a main component, as shown in
<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000003"
TARGET="tjitemdrw">drawing 1</A>
.

[0021]

DSP11 performs IP (interlace/progressive) conversion which changes the picture signal by the image source into a progressive signal from an interlace signal based on the parameter by the control system which is not illustrated.
DSP11 about Rhine without the data in the case of IP conversion changed into a progressive signal from an interlace signal
Motion detection performed when creating interpolation data is performed based on the data and the motion detection result of the front field which were interpolated and created from the present field, the data of 2 field delay, and the data of 1 field delay.
The field currently moved is interpolated in the field from the data of 1 field delay, and creates interpolation data, and a stationary field is interpolated between the fields from the data of the present field, and creates interpolation

data.
And the result of the interpolation in the field, and when the result of interpolation between the fields exceeds a certain threshold so that it may mention later, DSP11 regards it as a motion field, and performs interpolation in the field.
Moreover, DSP11 adjusts a threshold according to the result of motion detection of the front field.
A threshold will be made small, if the motion detection result of the front field is quiescence, and a threshold will be enlarged and it will specifically come to move.

[0022]

The memory 12 (M1) and 13 (M2) for generating the delay for the 1 field is arranged in the image entry-of-data stage of DSP11.
Image entry-of-data Rhine is connected to the input terminal of memory 12, and the 1st input terminal (I1) of DSP11.
The output terminal of memory 12 is connected to the input terminal of memory 13, and the 2nd input terminal (I2) of DSP21.
And the output terminal of memory 13 is connected to the 3rd input terminal (I3) of DSP.

[0023]

DSP11 is SIMD (Single Instruction Stream Multiple Data stream) which made many juxtaposition the linear array (line type array) mold DSP, for example, an element processor, in one dimension. It is constituted by the parallel processor of a control system.

[0024]

Below, about the concrete contents of processing of the concrete configuration of a SIMD control processor, and IP transform processing in DSP11, it relates with a drawing and order is explained later on.

[0025]

The configuration of a SIMD control processor is associated and explained to
<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000004"
TARGET="tjitemdrw">drawing 2</A>
below the fundamental configuration of a SIMD control processor.
This SIMD control processor 100 is constituted by the input pointer (input skip register) 101, the input SAM (serial access memory) section (input register) 102, the data memory section (local memory) 103, the ALU (Arithmetic and Logic Unit) array section 104, the output SAM section (output register) 105, the output pointer (output skip register) 106, and the program control section 107 as shown in
<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000004"
TARGET="tjitemdrw">drawing 2</A>
.

[0026]

The input SAM section 102, the data memory section 103, and the output SAM section 105 mainly consist of memory among these components.
The input SAM section 102, the data memory section 103, the ALU array section 104, and the output SAM section 105 constitute the element processor 110 of plurality (H or more [Several pixels for 1 horizontal-scanning period of a subject-copy image]) parallelized by the linear array (linear array) format.
the element processor 110 -- it has the component of the processor which became independent, respectively (single element), and corresponds to the part which attaches and shows a slash in
<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C

%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000004"
TARGET="tjitemdrw">drawing 2</A>

.
Moreover, two or more element processors 110 are arranged by juxtaposition in a longitudinal direction in
<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000004"
TARGET="tjitemdrw">drawing 2</A>
, and constitute an element processor group.

[0027]

The input pointer (input skip register) 101
By shifting the 1-bit signal [an input pointer signal (SIP)] of a logical value 1 (H), whenever it is 1 bit-shift register and the pixel data for 1 pixel of a subject-copy image are inputted from an external image-processing device (not shown) etc.
The element processor 110 which takes charge of the inputted pixel data for 1 pixel is specified, and the pixel data of the subject-copy image corresponding to the input SAM section 102 (input SAM cel) of the specified element processor 110 are written in.

[0028]

That is, the input pointer 101 makes the input pointer signal over the element processor 110 at the left end of
<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000004"
TARGET="tjitemdrw">drawing 2</A>
a logical value 1 first for every 1 horizontal-scanning period of a subject-copy image.
The pixel data of the first subject-copy image inputted according to the clock signal which synchronized with pixel data
It writes in the input SAM section 102 of the element processor 100 at the left end of the SIMD control processor 100 shown in
<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000004"
TARGET="tjitemdrw">drawing 2</A>

.
the input pointer signal of the logical value [as opposed to / whenever a clock signal furthermore changes by one period after that / the element processor 110 on the right one by one] 1 -- the method of the right -- shifting -- the element processor 110 -- every 1 pixel of image data of a subject-copy image is written in each input SAM section 102, and it dies.

[0029]

The input SAM section (input register) 102 memorizes the pixel data for 1 pixel (input data) inputted into an input terminal DIN from an external image-processing device etc., when the input pointer signal inputted from the input pointer 101 becomes a logical value 1, as mentioned above.
That is, the input SAM section 102 of the element processor 110 memorizes the pixel data for 1 horizontal-scanning period of a subject-copy image for every horizontal scanning period as a whole.
Furthermore, the input SAM section 102 transmits the pixel data (input data) of the subject-copy image for memorized 1 horizontal-scanning period to the data memory section 103 in the next horizontal scanning fly-back-line period if needed according to control of the program control section 107.

[0030]

The data memory section (local memory) 103 memorizes the pixel data of the subject-copy image inputted into the input SAM section 102, the data in the middle of an operation, a constant data, etc. according to the logical value of the input pointer signal (SIP) inputted from the input pointer 101 according to control of the program control section 107, and outputs them to the ALU array section 104.

[0031]

The ALU array section 104 performs arithmetic operation processing and logical operation processing to the pixel data of the subject-copy image inputted from the data memory section 103, the data in the middle of an operation, a constant data, etc. according to control of the program control section 107, and memorizes them to the predetermined address of the data memory section 103.
In addition, the ALU array section 104 performs all data processing to the pixel data of a subject-copy image by bitwise, and carries out data processing of the data for 1 bit for every cycle.

[0032]

The output SAM section (output register) 105 receives and memorizes a transfer of a processing result from the data memory section 103, when the processing currently assigned at 1 horizontal-scanning period is completed according to control of the program control section 107.
Moreover, the output SAM section 105 outputs outside the data memorized according to the output pointer signal (SOP) inputted from the output pointer 106.

[0033]

The output pointer (output skip register) 106 is constituted by 1 bit-shift register, activates an output pointer signal (SOP) alternatively to the output SAM section 105, and controls the output of a processing result (output data).

[0034]

The program control section 107 consists of ADORESUKO data (neither is illustrated) "low (ROW) one" for memory which constitute the sequence control circuit which controls advance of the program memorized by program memory and program memory and the input SAM section 102, the data memory section 103, and the output SAM section 105.
The program control section 107 performs processing to image data by interlocking and controlling all the element processors 110 by these components through the various control signals which generated and generated various control signals based on the single program which memorized the single program and was memorized for every horizontal scanning period of a subject-copy image.
Thus, it calls it SIMD control to control two or more element processors based on a single program.

[0035]

each pixel data of the subject-copy image which each element processor (processor element) 110 is a 1-bit processor, and is inputted from the circuit of an external image-processing device or the preceding paragraph -- receiving -- logical operation processing and arithmetic operation processing -- carrying out -- the element processor 110 -- it is based on an FIR digital filter as a whole -- filtering processing of horizontal and a perpendicular direction etc. is realized.
In addition, since SIMD control by the program control section 107 is performed considering a horizontal scanning period as a period, each element processor 110 can perform the program of the number of steps obtained by doing the division of max and the horizontal scanning period with the period of the instruction cycle of the element processor 110 for every horizontal scanning period.

[0036]

Moreover, it connects with the adjoining element processor 110, and the element processor 110 has the function to perform the adjoining element processor 110 and interprocessor communication, if needed.
That is, by being able to process according to SIMD control of the program control section 107 by accessing the data memory section 103 grade of the element processor 110 of right-hand or left-hand, and repeating access to the element processor 110 on

the right, each element processor 110 can access the element processor 110 to the data memory section 103 of the element processor 110 by which direct continuation is not carried out, and can read data.
The element processor 110 realizes horizontal filtering processing as a whole using the communication facility of contiguity interprocessor.

[0037]

Although a program step will increase very much if interprocessor communication is performed when data processing between the pixel data which left about 10 pixels is horizontally needed here, data processing to the pixel data which continue hardly including data processing between the pixel data which left no less than 10 pixels of actual FIR filtering is almost the case.
Therefore, the program step of FIR filtering which performs interprocessor communication increases, and it cannot hardly become non-efficiency.

[0038]

Moreover, each element processor 110 always takes charge of and processes the pixel data of the same location in the direction of a horizontal scanning specially.
Therefore, since the write-in address of the data memory section 103 of the point which transmits the pixel data (input data) of a subject-copy image from the input SAM section 102 can be changed for every early stages of a horizontal scanning period and the input data of the past horizontal scanning period can be held, also perpendicularly, the element processor 110 can filter the pixel data of a subject-copy image.

[0039]

in addition, the element processor 110 -- the input process (1st processing) which writes the pixel data (input data) of the subject-copy image which boils, respectively and can be set in the input SAM section 102 --
The transfer processing to the data memory section 103 of the input data memorized by the input SAM section 102 according to control of the program control section 107,
Data processing by the ALU array section 104, transfer processing (2nd processing) of the processing result (output data) to the output SAM section 105, and output processing (3rd processing) of the output data from the output SAM section 105 are performed in the pipeline format which made the processing period 1 horizontal-scanning period.
Therefore, when its attention is paid to input data, since the 1st to the same input data - each 3rd processing require the processing time for 1 horizontal-scanning period, the processing time for 3 horizontal-scanning period is needed by termination from initiation of these three processings.
However, since these three processings are performed in parallel in a pipeline format, if it averages, only the processing time for 1 horizontal-scanning period is needed for processing of the input data for 1 horizontal-scanning period.

[0040]

Hereafter, fundamental actuation of the linear array mold SIMD control processor for image processings shown in
<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000004"
TARGET="tjitemdrw">drawing 2</A>
is explained.

[0041]

With the input pointer 101, the element processor 110 to which a sequential shift is carried out, and the input pointer signal of the logical value 1 over each element processor 110 (H) takes charge of and carries out data processing of each pixel data of a subject-copy image is specified in the first horizontal scanning period (1st horizontal scanning period) according to the clock which synchronized with the pixel data of the inputted subject-copy image.

[0042]

The pixel data of a subject-copy image are inputted into the input SAM section 102 through an input terminal DIN.
In the input SAM section 102, the pixel data for 1 pixel of a subject-copy image are memorized by each element processor 110 according to the logical value of an input pointer signal.
In all the input SAM sections 102 of the element processor 110 corresponding to each pixel contained at 1 horizontal-scanning period, the pixel data of a subject-copy image are memorized, respectively.
And if the pixel data for 1 horizontal-scanning period are memorized as a whole, input process (1st processing) will be completed.

[0043]

After input process (1st processing) is completed, for every horizontal scanning period, according to a single program, SIMD control of the input SAM section 102, the data memory section 103, the ALU array section 104, and the output SAM section 105 of each element processor 110 is carried out by the program control section 107, and processing to the pixel data of a subject-copy image is performed.

[0044]

That is, in the next horizontal scanning fly-back-line period (2nd horizontal scanning period), each pixel data (input data) of the subject-copy image memorized in the 1st horizontal scanning period is transmitted to the data memory section 103 in each input SAM section 102.

[0045]

In addition, the program control section 107 accesses this data transfer processing by activating an input SAM read-out signal (SIR) [a logical value 1 (H)], and choosing the low (ROW) predetermined data of the input SAM section 102.
Furthermore, a memory access signal (SWA) is activated and it realizes by controlling the input SAM section 102 and the data memory section 103 to write the accessed data in the low predetermined memory cell (after-mentioned) of the data memory section 103.

[0046]

Next, based on a program, each element processor 110 is controlled by the program control section 107, and data are outputted to a horizontal scanning period from the data memory section 103 to the ALU array section 24.
In the ALU array section 104, arithmetic operation processing and logical operation processing are performed, and a processing result is written in the predetermined address of the data memory section 103.
After the arithmetic operation processing and logical operation processing according to a program are completed, in the program control section 107, control of the data memory section 103 is performed and a processing result is further transmitted to the output SAM section 105 at the next horizontal scanning fly-back-line period (the 2nd processes [this]).
Furthermore, in the next horizontal scanning period (3rd horizontal scanning period), the output SAM section 105 is controlled and a processing result (output data) is outputted outside (3rd processing).

[0047]

That is, in the next horizontal scanning period, if needed, the input data for 1 horizontal-scanning period memorized by the input SAM section 102 is transmitted to the data memory section 103, is memorized, and is used for the processing in a subsequent horizontal scanning period.

[0048]

Next, it relates and concrete processing of IP conversion in DSP11 which has a basic configuration as shown in
<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000004"

TARGET="tjitemdrw">drawing 2</A>
is explained to
<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000004"
TARGET="tjitemdrw">drawing 2</A>
-
<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000008"
TARGET="tjitemdrw">drawing 6</A>
.

[0049]

As shown in
<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000004"
TARGET="tjitemdrw">drawing 2</A>
and
<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000005"
TARGET="tjitemdrw">drawing 3</A>
, the interlace signal from the image source is inputted into the 1st input terminal I1 of DSP11 while it is inputted into memory 12 (this data is set to DI1).
Moreover, the data stored in memory 12 are inputted into the 2nd input terminal I2 of DSP11 while they are inputted into memory 13 (this data is set to DI2).
Furthermore, the data stored in memory 13 are inputted into the 3rd input terminal I3 of DSP11 (this data is set to DI3).
And the data memory section (
<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000004"
TARGET="tjitemdrw">drawing 2</A>
, 103) data DI 2 of DSP11 are stored by two lines.
These data are set to L1 and L2 (ST101, ST102).

[0050]

The data of data DI 1 and data DI 3 are compared, and the 1st absolute value of the difference is calculated (ST103), and when the 1st absolute value is below the 1st threshold (threshold 1) set up beforehand, it is considered that the pixel is a "quiescence field."
On the other hand, the data of data DI 1 and data DI 3 are compared, and the 1st absolute value of the difference is calculated (ST103), and when the 1st absolute value is larger than a setting threshold, it is considered that the pixel is a "motion field."

[0051]

If the result of motion detection of the above front field "quiescence" Becomes, a certain constant will be added to the 2nd threshold (threshold 2) (ST104), and if the result of motion detection of the front field "motion" Becomes, a certain constant will be subtracted to this threshold 2 (ST105).
It is made 128, when this threshold 2 exceeds 255, makes it 255 (ST106-ST108) and becomes small from 128 (ST109-ST111).
However, it is the case of 8 bits.

[0052]

The data of data DI 1 and data DI 3 are compared. And in the case of one or less threshold
As shown in
<A HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000006" TARGET="tjitemdrw">drawing 4</A>
, the interpolation data R1 in the field which are the average value of L1 and L2 data are created (ST112).
The field interpolation data R2 which are the average value of data DI 1 and DI3 data are created (ST113), the interpolation data R1 in the field are compared with the field interpolation data R2, and the 2nd absolute value of the difference is calculated (ST114).

[0053]

When the 2nd absolute value is larger than a threshold 2, it considers that the pixel is a "motion field", and when other, it is considered that the pixel is a "quiescence field."
and the space of a motion field -- being large -- it carries out (ST115).
In "a motion", the result of motion detection of an adjacent pixel considers the result of motion detection of its pixel as a motion.

[0054]

Consequently, from the data L1 and L2 stored in the internal memory according to the detection result, the pixel it was considered that was a "motion field" creates the interpolation data R1, and outputs the interpolation data R1 and data DI 2 (ST116, ST117).
On the other hand, the pixel it was considered that was a "quiescence field" outputs data DI 1 and data DI 2 (ST118).

[0055]

As mentioned above, when the result of the interpolation in the field and the result of interpolation between the fields exceed a predetermined threshold in this operation gestalt, it is regarded as a motion field and is made to consider as the interpolation in the field.
Consequently, when processing shown by
<A HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000012" TARGET="tjitemdrw">drawing 10</A>
(A) - (D) is performed, as shown in
<A HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000007" TARGET="tjitemdrw">drawing 5</A>
(A), an error does not occur.
When similarly processing shown by
<A HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000013" TARGET="tjitemdrw">drawing 11</A>
(A) - (D) is performed, as shown in
<A HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000007" TARGET="tjitemdrw">drawing 5</A>
(B), an error does not occur.

[0056]

Furthermore, although the black-lacquered rectangular head (**) of 1 field eye and 3 field eye is standing it still in the same location with the still picture as shown in the above-mentioned algorithm in the case of a still picture (C) with 1ON/1OFF (for example,
<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000008"
TARGET="tjitemdrw">drawing 6</A>
(A) -)
When it is over the white round head (O) equivalent to the same location interpolated and created from the rectangular head (**) of the void of 2 field eye, and the threshold which the difference of the data of a black-lacquered rectangular head (**) set up
Since it will be regarded as a motion in spite of standing it still originally, the data interpolated in the field of 2 field eye will be outputted as a result.
Consequently, an image may flicker.
Then, in this operation gestalt, as mentioned above, the result of motion detection of the front field adjusts this threshold automatically.
And it will be made low, if the result of motion detection of the front field is quiescence, and this threshold will be made high and it will come to move.
Under the present circumstances, it is made for a threshold not to come out of a certain within the limits.
Thereby, when quiescence continues, a threshold becomes higher and higher, and when above, IP conversion can be performed that there is nothing with rice cake.

[0057]

As explained above, according to this operation gestalt, about Rhine without the data in the case of IP conversion changed into a progressive signal from an interlace signal
Motion detection performed when creating interpolation data is performed based on the data and the motion detection result of the front field which were interpolated and created from the present field, the data of 2 field delay, and the data of 1 field delay.
Interpolate the field currently moved in the field from the data of 1 field delay, it creates interpolation data, and a stationary field
When it interpolates between the fields from the data of the present field, interpolation data are created and the result of the interpolation in the field and the result of interpolation between the fields exceed a certain threshold
Since DSP11 which makes a threshold small was formed when regarding it as the motion field, performing interpolation in the field, the motion detection result of the front field was quiescence, and enlarging the threshold and coming to move
the breakdown of the motion detection generated in case IP conversion of the screen of high-speed scrolling is carried out -- mitigable -- precision -- IP conversion can be performed highly.

[0058]

[Effect of the Invention]

even if it performs IP conversion to the image accompanied by high-speed scrolling according to this invention -- the breakdown of motion detection -- few -- it can interpolate -- precision -- there is an advantage which can perform IP conversion highly.

<HR>DESCRIPTION OF DRAWINGS
<HR>[Brief Description of the Drawings]

<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000003"
TARGET="tjitemdrw">[Drawing 1]</A>

It is the block diagram showing 1 operation gestalt of the picture signal processor concerning this invention.

<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000004"
TARGET="tjitemdrw">[Drawing 2]</A>

It is the block diagram showing the fundamental configuration of the SIMD control processor which constitutes DSP concerning this invention.

<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000005"
TARGET="tjitemdrw">[Drawing 3]</A>

It is a flow chart for explaining actuation of the picture signal processor concerning this invention.

<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000006"
TARGET="tjitemdrw">[Drawing 4]</A>

It is a flow chart for explaining actuation of the picture signal processor concerning this invention.

<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000007"
TARGET="tjitemdrw">[Drawing 5]</A>

It is drawing showing the result of IP conversion at the time of processing
<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000012"
TARGET="tjitemdrw">drawing 10</A>
(A) - (D) and
<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000013"
TARGET="tjitemdrw">drawing 11</A>
(A) - (D) in the picture signal processor concerning this invention.

<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000008"
TARGET="tjitemdrw">[Drawing 6]</A>

It is drawing for explaining the effectiveness by adjusting this threshold automatically by the result of motion detection of the front field.

<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000009"
TARGET="tjitemdrw">[Drawing 7]</A>

It is an interlace signal-description Fig.

<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl

l.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000010"
TARGET="tjitemdrw">[Drawing 8]</A>

It is a progressive signal-description Fig.

<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000011"
TARGET="tjitemdrw">[Drawing 9]</A>

It is the explanatory view of IP conversion.

<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000012"
TARGET="tjitemdrw">[Drawing 10]</A>

It is drawing for explaining the technical problem of the conventional IP conversion.

<A
HREF="http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web_cgi_ejje?u=http%3A%2F%2Fwww4.ipdl.inpit.go.jp%2FTokujitu%2Ftjitemdrw.ipdl%3FN0000%3D237%26N0500%3D1E%5FN%2F%3B%3E%3C%3C%3C696%3B%2F%2F%2F%26N0001%3D626%26N0552%3D9%26N0553%3D000013"
TARGET="tjitemdrw">[Drawing 11]</A>

It is drawing for explaining the technical problem of the conventional IP conversion.

[Description of Notations]

10 [-- A SIMD control processor, 101 / -- An input pointer (input skip register), 102 / -- The input SAM section (input register), 103 / -- The data memory section (local memory) 104 / -- The ALU array section, 105 / -- The output SAM section (output register), 106 / -- Output pointer (output skip register).] -- A picture signal processor, 11 -- 12 DSP, 13 -- Memory, 100

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